REMARKS

Claims 10-24 are pending in the present application, claims 18-24 having been added herein. The Office Action and cited references have been considered. Favorable reconsideration is respectfully requested.

The drawings were objected to for failing to show the memory controller, the nonvolatile memory, and the internal volatile flag memory, and the relationship between the elements. Applicant is submitting herewith a new figure 3 showing those elements, and the relationship between them. The specification has been amended to provide an explicit description. Applicant respectfully submits that no new matter has been added, because the illustrated elements and the relationship between them, is supported by the specification as originally filed. Approval of the new drawing is respectfully requested.

The claims were rejected under 35 U.S.C. § 112, second paragraph, as failing to conform to U.S. practice. Applicant has amended the claims to overcome this rejection. Applicant submits that these amendments do not affect the scope of the claims, and are not intended to be, nor are they narrowing amendments. Withdrawal thereof is respectfully requested.

Claims 10-17 were rejected under 35 U.S.C. §102 (b) as being anticipated by Larner et al. (U.S. Patent No. 6,104,638). This rejection is respectfully traversed for the following reasons.

Claim 10 has been rewritten to include one of the limitations previously recited in claim 13. In particular, Claim 10 now recites a method for reconstructing

administrative data records relating to a nonvolatile memory that can be written in units of sectors and erased in units of blocks, the administrative data records being stored in an internal volatile flag memory of an assigned memory controller. The method comprising the steps of setting up, in one or more memory blocks of the nonvolatile memory, a contiguous reconstruction table for administrative memory data (RKT), continually updating the reconstruction table in the nonvolatile memory with administrative data records relating to all write and erase operations out of the internal volatile flag memory, the step of continually updating comprising recording all information with which the administrative data records of the internal volatile flag memory of the memory controller can be completely reconstructed during a restart after a power failure, starting a reconstruction when a predefined fill level of the reconstruction table (RKT) is reached, to create a defined initial state of the administrative data records in the internal volatile flag memory and in the reconstruction table (RKT), recording the start of the reconstruction as a last entry (OE) in the reconstruction table, and recording a completion entry (FE) into the reconstruction table, every time the reconstruction was successful. This is not taught, disclosed or made obvious by the prior art of record.

The remarks submitted in the amendments filed on April 26, 2007, November 7, 2007, and October 9, 2007, are incorporated by reference herein. In addition, Applicant submits the following remarks.

Larner describes a processor system with a RAM and a non-volatile memory, which is arranged in individually erasable segments, also called blocks. The patent relates to a method to synchronize the values of administrative data words (parameters) in the

RAM with previously updated data words which were continuously written to at least two reserved segments of the non-volatile memory. At the beginning of a segment, a special ID with a counter value is written, and the end of the relevant data entries is found by an entry that has the value of an erased memory location. The synchronizing is done by reading all relevant entries and overwriting the corresponding memory location in the RAM until an empty (erased) entry is found. As the first segment is filled up, the second segment is filled with current data words from RAM and the first segment is erased and filled with the value FFFFhex. The next updating is done in the second segment until this is filled up again. Then the segments are swapped again.

Applicant's application also relates to a method to update memory locations in RAM from a reconstruction table in the non-volatile memory. One difference between the claimed invention and Larner lies in the method for the reconstruction of the table and which types of entries for which the method is utilized. According to Applicant's invention, the reconstruction table has a fixed length and is optimized for memory administration data. On page 12, the Office notes that claim 10 does not recite that the reconstruction table is fixed length and is optimized for memory administration. Applicant agrees, and asserts that the argument previously presented was made without deceptive intent, but was merely made to explain the invention with respect to all of the claims, not just the independent claims. The feature of the fixed length table was meant to refer to the recitation of claim 11 that "every entry in the reconstruction table (RKT) is one sector or one sector segment long", which depends from claim 10. As for the optimization, this is

inferentially claimed in claim 10 since claim 10 recites that the method includes "setting up,... a contiguous reconstruction table for administrative memory data (RKT)." Applicant regrets these misunderstandings. Applicant has added new claim 18 that includes these two features specifically recited therein.

Further, according to the present invention, there are tables holding the relation between logical and physical addresses and the addresses of alternate sectors, to which data is written until a sector is filled. These tables of memory administration data can be brought into a defined state that corresponds to the state used at the initial start of the memory system. As mentioned in the previous response, when the entries fill up the reconstruction table, a reorganization is started which brings the memory administration data into the defined state. This start is marked with a special start-entry (OE). The Office asserts on page 12 that the reorganization feature argued here is not recited in claim 10. Applicant respectfully disagrees. Claim 10 recites "starting a reconstruction when a predefined fill level . . . is reached . . . [and] recording the start of the reconstruction as a last entry (OE). . . ." One of ordinary skill would understand that this argument concerning reorganization refers to the claimed start of a reconstruction.

As also mentioned in the previous response, the end of the reorganization process is also marked with a special end-entry (FE). If the end-entry (FE) is encountered, all entries before that are no longer relevant. Page 12 of the Office Action also asserts that the end-entry is not recited in claim 10. Applicant agrees, and again asserts that the argument previously presented was made without deceptive intent, but was merely made

to explain the invention with respect to all of the claims, not just the independent claims. However, Applicant has amended claim 10 to include recording a completion entry (FE), *i.e.*, the end-entry.

In Larner, there is no reorganization process to bring the administrative data into a defined initial state. Larner only describes a reconstruction process to synchronize the values in the RAM and in the reconstruction table to the same current values. The administrative data of Larner do not have a defined initial state. They tend to become larger and larger. The claimed invention anticipates initial states of the data, such as initial values in allocation tables for memory addresses. The reorganization process brings the data into defined initial states which correspond to a new memory. Such a reorganization is marked with special entries in the reconstruction table. This is different than the end-of-table (FFFFhex). Both methods have such an end-of-table value behind the last written entry. Larner does not use a reorganization (reconstruction) and so there is no start-of reorganization marker (OE). Claim 10 also includes recording a completion marker for the successful reorganization (FE). Both markers are not taught or suggest in Larner.

According to the present claimed invention, the reorganization of the reconstruction table is not done by reading the actual values of the parameters from RAM. The reorganization is done by bringing the administrative memory data into an initial state and marking this process in the reconstruction table with the different entries FE and OE. This reorganization is not anticipated by Larner, as Larner teaches only an end-of-table-

marker (FFFFhex) and a counter at the beginning of the table, which is not sufficient for the reorganization process.

In view of these differences, Applicant respectfully submits that Larner does not disclose Applicant's claimed invention arranged as in claim 10. Applicant further submits that claims 11-17 are patentable at least for the reasons discussed above with respect to claim 10.

In the Office Action, the Examiner asserted that the arguments based on the lack of reorganization in the prior art do not have basis in the claims. Without conceding the merits of this assertion, Applicant has added new claims 18-24, which specifically recite a reorganization step (instead of the term "reconstruction" of claims 10-17). Applicant respectfully submits that claims 18-24 are patentable for the reasons discussed above with respect to claims 10-17.

In the view of the above amendment and remarks, Applicant respectfully submits that claims 10-24 are patentable over the prior art of record. Applicant requests reconsideration and withdrawal of the outstanding rejections of record. Applicant submits that the application is now in condition for allowance and early notice to this effect is most earnestly solicited.

If the Examiner has any questions, he is invited to contact the undersigned at 202-628-5197.

Respectfully submitted,

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